Motivation

- The quality of 2G HTS wire depends on the process stability at each fabrication step. Advanced monitoring and control techniques help drastically improve the $I_c$ uniformity along the wire length.
- To simplify buffer layer architecture is promising for increasing production throughput, provided that it leads to no degradation in the finished wire performance.
- Optimal cost/performance of the wire is a complex function of multiple parameters, including $I_c$, piece length and HTS layer thickness.

Buffer texture quality monitoring

**Better $I_c$ performance by improved buffer texture control**

Determine optimal window of texture factor

Implement automated closed-loop control

**Higher throughput by simplified buffer architecture. No loss in wire quality.**

20% Throughput increase without $I_c$ degradation by eliminating CeO$_2$ cap layer

Adhesion strength measurements by climbing drum peel test

**Wire cost management: HTS layer thickness / $I_c$ / piece length**

Statistical data for a representative set of wires. NOTE: assuming $50/m cost.

**Summary**

- We implemented automated closed-loop control of buffer deposition process. It maintains the texture quality parameter within an optimal window thus improving the $I_c$ level and uniformity.
- We simplified the buffer layer architecture by eliminating the CeO$_2$ cap layer. This resulted in a 20% throughput increase, without any degradation of wire properties.
- At present, for cost/performance considerations, we make 1.5 mm-thick HTS layer delivering 500-600 A/12 μm width.